

CLAIMS

- 1 1. A circuit arrangement for transferring data between a data transmitter and a data receiver,
2 said circuit arrangement comprising:
3 a buffer device that receives a data signal from the data transmitter and provides a buffered
4 data signal onto a data bus;
5 a first memory element that receives and stores said buffered signal on said data bus and
6 provides a first stored signal;
7 a second memory element that receives and stores said first stored signal and provides a
8 second stored signal to the data receiver; and
9 a controller that controls the output state of said buffer device, to control the transfer of
10 data from said first memory element to said second memory element.
- 1 2. The circuit arrangement of claim 1, wherein said first memory element comprises by
2 inherent parasitic capacitance associated with said data bus.
- 1 3. The circuit arrangement of claim 1, wherein said first memory device is constructed as a
2 capacitive element, one of whose terminals is connected to said data bus , and whose other
3 terminal is connected to a reference potential.
- 1 4. The circuit arrangement of claim 3, wherein capacitance of said capacitive element is

2 provided by the line capacitance of said data bus with respect to one or more reference lines.

1 5. The circuit arrangement of claim 2, wherein said first memory device comprises a
2 dedicated memory element that comprises a holding element.

1 6. The circuit arrangement of claim 3, wherein said controller controls said data buffers (P1,
2 P2) associated with the data transmitter (S) and the data receivers (E), and the second memory
3 devices (Sp2).

1 7. The circuit arrangement of claim 1, wherein said controller comprises:
2 a first control section, associated with the data transmitter, for controlling the first data
3 buffer; and
4 a second control section, associated with each of the data receivers, that controls second
5 data buffers and said second memory devices, a control data communication between the data
6 transmitter and the data receiver.

1 8. The circuit arrangement of claim 7, wherein at least one of the circuit sections (1, 2) is part
2 of a peripheral region (2) of the integrated circuit for accepting the connection pads of the
3 input/output connections.

1 9. The circuit arrangement of claim 1, wherein the circuit arrangement has at least one

2 microprocessor/microcontroller and/or at least one signal processor with a given set of states.

1 10. The circuit arrangement of claim 1, wherein said first memory element consists of
2 parasitic capacitance associated with said data bus.

1 11. An integrated circuit arrangement for transferring data between a data transmitter and a
2 data receiver, said circuit arrangement comprising:

3 means for receiving a data signal from the data transmitter and for providing a buffered
4 data signal onto a data bus;

5 a first memory element that receives and stores said buffered signal on said data bus, and
6 provides a first stored signal;

7 a second memory element that receives and stores said first stored signal, and provides a
8 second stored signal to the data receiver; and

9 a controller that controls the output state of said means for receiving, such that when said
10 means for receiving provides a high impedance output data is transferred from said first memory
11 element to said second memory element.